REMARKS

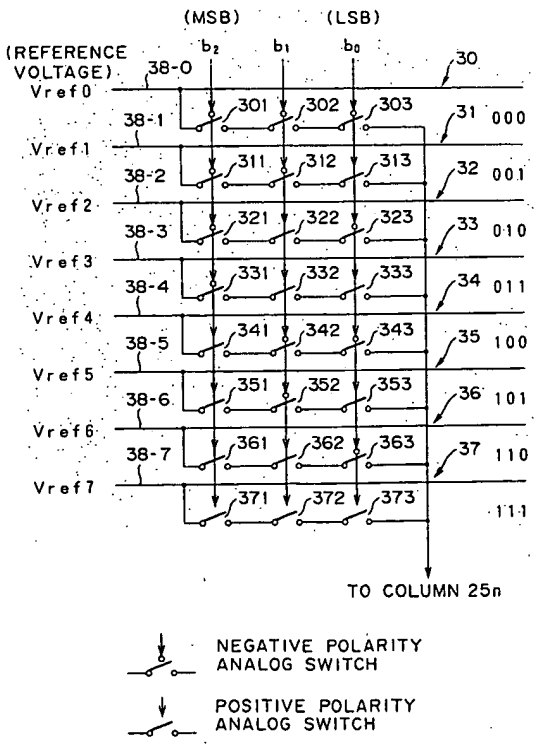
This amendment is in response to the Official Action dated December 20, 2007. Claims 59-63 have been added; as such claims 1-3, 10-25, 40-45, 54-63 are now pending in this application. Claims 1, 10, 17, 40, and 54 are independent claims. Reconsideration and allowance is requested in view of the claim amendments and the following remarks.

Support for the new claims can be found in Fig. 3 and the corresponding portion of the specification.

An example embodiment

Fig. 3 illustrates an example embodiment of a digital-to-analog (DAC) converter for a 3-bit signal in accordance with the present invention. The 3-bit values of the digital signal are input, from most significant bit to least significant bit (MSP-LSP), at input lines b2, b1, and b0. The digit signal is converted to one of eight step voltages Vref0-Vref7 ($2^3 = 8$ voltage values). Step select circuits 30-37 connect the eight step reference voltages to column output 25n. Each step select circuit includes three serially connected analog switches polarized to the corresponding input digital bit (b2 to b0). Step select circuit comprises a combination of positive and negative polarity switches such that for a corresponding digital value only a single reference voltage will connect to the column output 25n.

FIG. 3



Rejections under 35 U.S.C. § 102

Claims 1-3 have been rejected under 35 U.S.C. § 102 as anticipated over U.S Patent No. 6,911,926 to Koyoma et al. ("Koyoma").

Applicant traverses this rejection.

> Claim 1 recites: *[a] digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;*
>
> *wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area.*

With respect to claim 1, Koyoma fails to teach or suggest "*each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal.*"

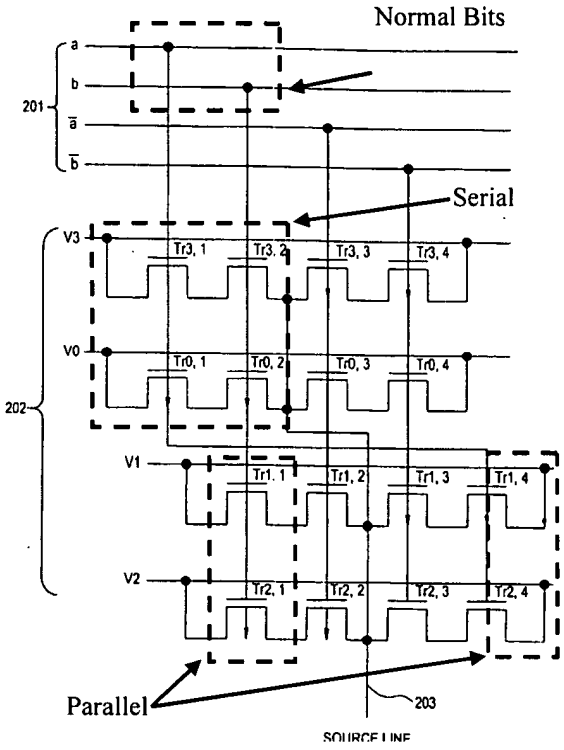
Claim 1 discloses a structure that applies to "*each step select unit*" in the digital-to-analog converter must have the disclosed structure. Furthermore, with respect to the identified analog switches, claim 1 recites "*n serially connected analog switches*".

Fig. 2 (below) of Koyoma illustrates a digital-to-analog converter for a 2-bit signal. The 2-bit signal is input via four lines 201, i.e., 2 normal lines (a & b) and 2 inverse lines ($\bar{a}$ & $\bar{b}$). Each step select circuit includes 4 switches corresponding to the 4 input lines comprising 2 p-type TFTS (left) and 2 n-type TFTs (right). This illustrates that in Koyoma an n-bit signal requires 2n switches in each step select unit.

By contrast, claim 1 recites "*each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal.*" Koyoma employs 2n switches for each step select unit, whereas clam 1 recites n switches.

Fig. 2 also illustrates 4 reference voltages V0-V3 corresponding to the 2^n possible reference voltage circuit corresponding to each value of the 2-bit signal. With respect to the step select circuits connected to V0 and V3, the switches corresponding to the normal bit signals (a & b) are connected serially, i.e., Tr3,1 & Tr3,2 for V3 and Tr0,1 and Tr0,2 for V0. However, with respect to V1 and V2, the switches corresponding to the normal bit signals (i.e., Tr1,1 and Tr1,4 for V1 and Tr2,1 and Tr2,4 for V2) are connected in *parallel*. As such, only the first two step select units for the DAC, have switches serially connected and polarized to match the state of each bit of the digital data signal. The remaining step select circuits have some serially connected switches and some switches in parallel and as such do not have all n polarized switches in serial.

FIG. 2



For example, in the step selected circuit for V3, switches Tr3,1 and Tr3,2 are polarized and serial; and in the step selected circuit for V0, switches Tr0,1 and Tr0,2 are polarized and serial; However, in the step selected circuit for V2, switches Tr1,1 and Tr1,4 are polarized, but are also in parallel; and in the step selected circuit for V2, switches Tr2,1 and Tr2,4 are polarized, but are also in parallel.

Therefore, if one were to take the position that polarized switches only refer to those switches that connect to the non-inverted, normal bit signals, (to overcome Applicant's prior argument) then Koyoma would fail to teach or suggest "*each step select unit including n serially connected analog switches polarized to match a logic state of each bit.*" The fact that Koyoma continually shifts the left most bit to the right side of the next step select unit, effectively causes the polarized switches to only be serially connected in the first pair of step select units. Furthermore, it would not be possible to create a DAC using Koyoma's architecture and limit it to only the first two step select units, because Koyoma and claim 1 clearly exclude 1-bit signals.

Alternatively, if one were to argue that all the switches in Koyoma are polarized, then Koyoma still fails to read on claim 1 because Koyoma 2n switches in each step select circuit and not n switches as recited in claim 1.

Furthermore, it would not be obvious to modify Koyoma because the arrangement of the switches is fundamental to the architecture that Koyoma introduces to the DAC. Particularly, Koyoma seeks to keep only p-type transistors on the left side of the DAC and n-type transistors on the right. This simplifies the construction of the Koyoma DAC. However, a drawback of this architecture is the need to rewire the left-most signal line (e.g., signal line a in Fig. 2) after each pair of step select circuit to the right most side of the next pair of step select circuit.

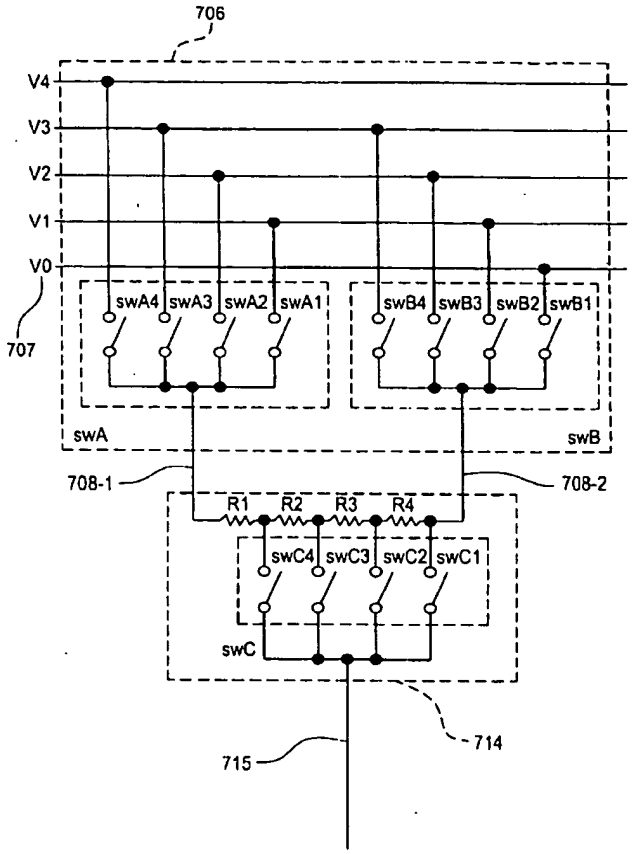
The Office Action cites to Col 4, line 60 – Col. 5, line 63 as the basis for rejecting the above-cited portions of claim 1. These portions of Koyoma discuss the configuration of the p-type and n-type transistors. These transistors are indeed connected serially. However, as set forth above, first, each of the step select circuits in Koyoma include *2n* switches, where claim 1 recite *n* switches per step select circuit. Furthermore, of the properly *polarized switches,* i.e., the switches connected to the non-inverted signals, only the first pair of step select circuit includes polarized switches in series, while claim 1 requires that all the polarized switches in every step select circuit be in series.

With respect to claim 1, Koyoma also fails to teach or suggest "*wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input of an effective pixel area.*"

Fig. 2 of Koyoma illustrates that both ends of the step select units comprising $Tr_{3,1}$, $Tr_{3,2}$, $Tr_{3,3}$, $Tr_{3,4}$, are connected to the same reference voltage line (V3), and it is the midpoint, not the "other end," of the step select unit that is connected to the source line.

The Office Action compares the "*digital-analog converter circuit*" in claim 1 to the DAC disclosed in Koyoma, citing to columns 25-26 of Koyoma, which describe Fig. 9. Fig. 9 of Koyoma provides a schematic of a D/A conversion circuit. Like the circuit from Fig. 2 of Koyoma described above, the DAC in Fig. 9 also fails to teach or suggest "*[a] digital-analog converter circuit ...*

comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal; wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line in effective pixel area."



(Fig. 9 of Koyoma)

First, Fig. 9 of Koyoma does not teach that "*each step select* ***unit including n serially connected analog switches*** *polarized to match a logic state of each bit of the n-bit digital data signal.*" As is evident, the switches are all connected in parallel to their respective reference voltages. Second, claim 1 recites that each step unit is connected to "*the reference voltage*", i.e., there is one reference voltage to which each step unit is connected. While in Koyoma, each switch is connected to its own reference voltage, such that the step select circuits in Fig. 9 are connected to a plurality of voltages. Finally, even if Fig. 9 did disclose that the switches were in serial, which

clearly they are not, Fig. 9 still fails to teach that one end of the step select units are all connected to the reference voltage lines and it is the midpoint of the step select unit, not the "other end," of the step select unit that would be connected to the source line.

Accordingly, Koyoma fails to teach or suggest at least these features of claim 1. Furthermore, at least for the reason disclosed above claims 2 and 3 overcome Koyoma because they depend on independent claim 1.

Accordingly, Applicant respectfully requests that the rejection of claims 1-3 under 35 U.S.C. § 102 be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 10-25, 40-45, and 54-58 have been rejected under 35 U.S.C. § 103 as obvious over Koyoma in view of U.S. Patent No. 6,274,869 to Butler et al. ("Butler").

Applicant respectfully traverses this rejection.

Claim 10 recites: *[a] liquid crystal display comprising:*

a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area;

and a level shift circuit for converting a low voltage amplitude signal to a high voltage amplitude signal comprising:

a CMOS latch cell having two input sections,

wherein a first resistor element is inserted between each of the two input sections and two signal sources.

As set forth above, Koyoma fails to teach or suggest, at least, "*a digital-analog converter ... comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal; wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area.*"

Butler is directed to an offset correction circuit for a focal point array. The offset correction circuit serves to correct for non-uniformity among sensor element output. This ensures that when a plurality of sensors is used in an array, the output of various sensors can be normalized.

Butler does not disclose a "*a digital-analog converter circuit ... comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal; wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area.*"

Butler therefore fails to teach or suggest various features of independent claim 10. For similar reasons, Butler fails to teach or suggest various features of claims 17, 40, and 54. Furthermore, at least for the reason disclosed above claims 11-16, 18-25, 41-45, and 55-58 also overcome Butler because they depend on independents claims 10, 17, 40, and 54, respectively.

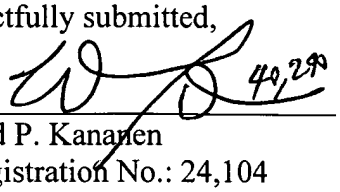
Accordingly, Applicant respectfully requests that the rejection of independent claim 10-25, 40-45, and 54-58 under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: February 6, 2008

Respectfully submitted,

By 

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